IN THE SPECIFICATION:

Please replace the paragraph beginning on page 8, line 21, with the following rewritten paragraph:

HDLC abort and flag check 80 analyzes the incoming bytes for start of frame, end of frame, and abort sequences. 0x7e values, indicating inter-frame time fill, are discarded until a non-0x7e value is received, indicating data. Data bytes are forwarded to HDLC descrambler 82.

Please replace the paragraph beginning on page 9, line 17, with the following rewritten paragraph:

29-bit shift register 120 is flushed out by every 29 bits of incoming scrambled data. An error in the bits of scrambled inter-frame time fill bytes causes the shift register to go out of synchronization with the transmitting end scrambler. The next runt abort packet, however, resynchronizes 29-bit shift register 120 by flushing any errors out of the shift register. Even though the runt abort packet will not be descrambled correctly when there is an error in 29-bit shift register 120, the runt abort packet will place the shift register in a correct state. Subsequent scrambled data will be descrambled correctly. This minimizes the impact that errors in inter-frame time fill bytes have on descrambling data.

Please replace the paragraph beginning on page 9, line 26, with the following rewritten paragraph:

Fig. 6 is a flow chart illustrating the processing performed by incoming HDLC processing element [[46]] 48. Incoming HDLC processing element [[46]] 48 first checks the incoming data for abort and flag information (step 100), descrambles the data (step 102), removes packets having a byte length less than six bytes (step 104), and performs FCS checking operations on the data (step 106). Each of the steps is described in greater detail in the description of Fig. 4.